AMENDMENTS TO THE DRAWINGS

"Annotated Sheets Showing Changes" are attached which include marked-up versions of Figures 1-5.

Attachment: Annotated sheet showing changes.

REMARKS

In response to the Office Action mailed June 4, 2007, Applicants respectfully request reconsideration. Claims 1 and 3-30 were previously pending in this application. By this amendment, claims 1, 7, 11, 13-15, 17-19 and 24-30 have been amended. As a result, claims 1 and 3-30 are pending for examination with claims 1, 24, 26 and 30 being independent. No new matter has been added.

Objections to the Drawings

The Office Action objected to the drawings under 37 CFR 1.83(a) as allegedly failing to show any functional description. Applicants have herein amended Figs. 1-5 to address the Examiner's concerns.

Accordingly, withdrawal of this objection is respectfully requested.

Rejections under 35 U.S.C. §112

The Office Action rejected claims 26, 27 and 30 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Applicants have amended claims 26-30 to address the Examiner's concerns. Support for these amendments can be found, for example, on page 5, lines 14-15 and on page 7, lines 26-20 – page 8, lines 1-9 of the specification.

Accordingly, withdrawal of this rejection is respectfully requested.

The Office Action also rejected claims 11, 15, 19, 26 and 30 under 35 U.S.C. 112, second paragraph, as being indefinite. Applicants have amended claims 11, 15, 19 and 26-30 to address the Examiner's concerns.

Accordingly, withdrawal of this rejection is respectfully requested.

Rejections Under 35 U.S.C. §103

I. The Office Action rejected claims 1, 3-9 and 13-25 under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis et al (U.S. Patent No. 5,797,043), hereinafter "Lewis," in view of George et al. (US Patent Number 6,785,829), hereinafter "George." Applicants respectfully disagree. In addition, Applicants have amended claims 1, 7, 13-15, 17-19, 24 and 25 to more clearly distinguish over the cited references.

Claim 1, as amended, recites:

> A processing system for accessing data, the processing system comprising:
>
> a processor comprising an execution unit for executing instructions;
>
> a stream register unit being part of the processor and configured to supply a first type of data to the execution unit, the first type of data being data supplied from a peripheral, the stream register unit including *at least one stream register unit FIFO* configured to store the first type of data received from the peripheral;
>
> a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO; and
>
> a memory bus, separate from the communication path, connected between a data memory and the processor, across which the processor can access a second type of data, the second type of data being randomly accessible data held in the data memory;
>
> *wherein the first type of data is supplied via the communication path directly from the FIFO coupled to the peripheral to the stream register unit of the processor and the second type of data is supplied via the memory bus, separate from the communication path, between the data memory and the processor.*
>
> (Emphasis added).

On page 6, the Office Action concedes that Lewis fails to teach a system wherein a stream register unit being part of the processor. The Office Action then alleges that George "teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3)." George discusses that "[c]ache 365 is a special memory subsystem that stores frequently accessed data and its memory locations for quick access by processor core 363." (George, col. 5, lines 49-51). However, George does not teach or suggest "the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral," as recited in claim 1. Furthermore, George does not teach or suggest "a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO," as recited in claim 1.

In view of the foregoing, claim 1 patentably distinguishes over Lewis and George, either alone or in combination.

Claims 3-23 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1 and 3-23 is respectfully requested.

Claim 24, as amended, recites:

A streaming data handling system, comprising:

a processor comprising an execution unit for executing instructions;

a stream register being part of the processor and configured to supply data from a peripheral to the processor, *the stream register including at least one stream register FIFO configured to store the data received from the peripheral*; and

a FIFO memory coupled to the peripheral to receive the data from the peripheral and connected to the least one stream register FIFO via a communication path,

wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order.

(Emphasis added).

On page 6, the Office Action concedes that Lewis fails to teach a system wherein a stream register unit being part of the processor. The Office Action then alleges that George "teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3)." George discusses that "[c]ache 365 is a special memory subsystem that stores frequently accessed data and its memory locations for quick access by processor core 363." (George, col. 5, lines 49-51). However, George does not teach or suggest "the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral," as recited in claim 24. Furthermore, George does not teach or suggest "a FIFO memory coupled to the peripheral to receive the data from the peripheral and connected to the least one stream register FIFO via a communication path," as recited in claim 24.

In view of the foregoing, claim 24 patentably distinguishes over Lewis and George, either alone or in combination.

Claim 25 depends from claim 24 and is allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 24 and 25 is respectfully requested.

II. The Office Action rejected claim 26-30 under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis in view of Garcia et al. (US Patent Number 6,433,785), hereinafter

"Garcia." Applicants respectfully disagree. In addition, Applicants have amended claims 26-30 to more clearly distinguish over the cited references.

Claim 26, as amended, recites:

A stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and a peripheral and comprising:

a receiver arranged to receive a request for a data item from the execution unit;

at least one FIFO configured to store the data item received from the peripheral; and

a stream engine, arranged to:

receive the request for the data item;

determine whether the requested data item is in the at least one FIFO;

if the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor; and

send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request.

(Emphasis added).

As discussed above, on page 6, the Office Action concedes that Lewis fails to teach a stream register unit being part of the processor. Similarly, Garcia does not teach or suggest "a stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and a peripheral and comprising: a receiver arranged to receive a request for a data item from the execution unit; at least one FIFO configured to store the data item received from the peripheral; and a stream engine …," as recited in claim 26.

Therefore, neither Lewis nor Garcia teaches or suggests all the limitations of claim 26.

In view of the foregoing, claim 26 distinguishes over the cited references and is in condition for allowance.

Claims 27-29 depend from claim 26 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 26-29 is respectfully requested.

Claim 30, as amended, recites:

A stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and a memory, the stream register comprising:

a receiver arranged to receive a request for a data item from the execution unit of the processor;

at least one FIFO configured to store the data item received from a peripheral; and

a stream engine, arranged to:

receive the request for the data item;

determine whether the requested data item is in the at least one FIFO;

if the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor; and

send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, if the data item is available, send the data item to the execution unit of the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request.

(Emphasis added).

As discussed above, on page 6, the Office Action concedes that Lewis fails to teach a stream register unit being part of the processor. Similarly, Garcia does not teach or suggest "a stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and a memory, the stream register comprising: a receiver arranged to receive a request for a data item from the execution unit of the processor; at least one FIFO configured to store the data item received from a peripheral; and a stream engine …," as recited in claim 30.

Therefore, neither Lewis nor Garcia teaches or suggests all the limitations of claim 30.

In view of the foregoing, claim 30 distinguishes over the cited references and is in condition for allowance.

Accordingly, withdrawal of the rejection of claim 30 is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: November 5, 2007

Respectfully submitted,

By: /James H. Morris/

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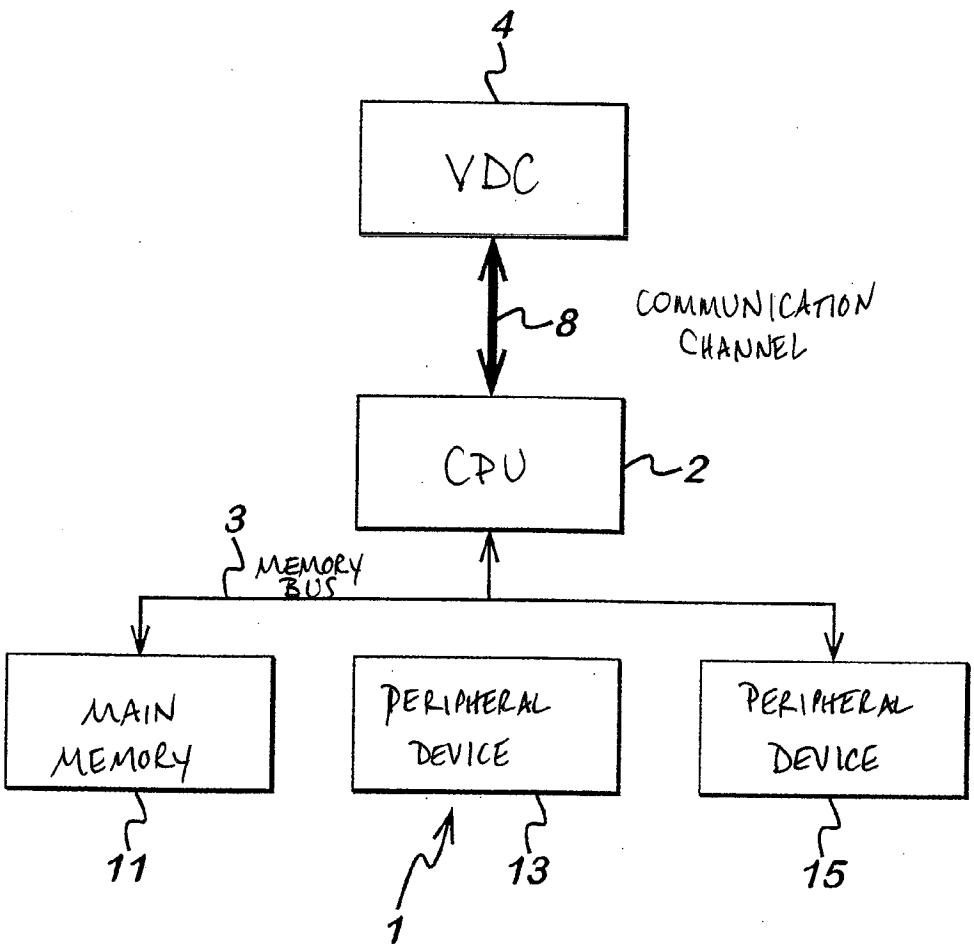
Fig. 1


4
VDC
8
COMMUNICATION CHANNEL
CPU
2
3
MEMORY BUS
MAIN MEMORY
PERIPHERAL DEVICE
PERIPHERAL DEVICE
11
1
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15

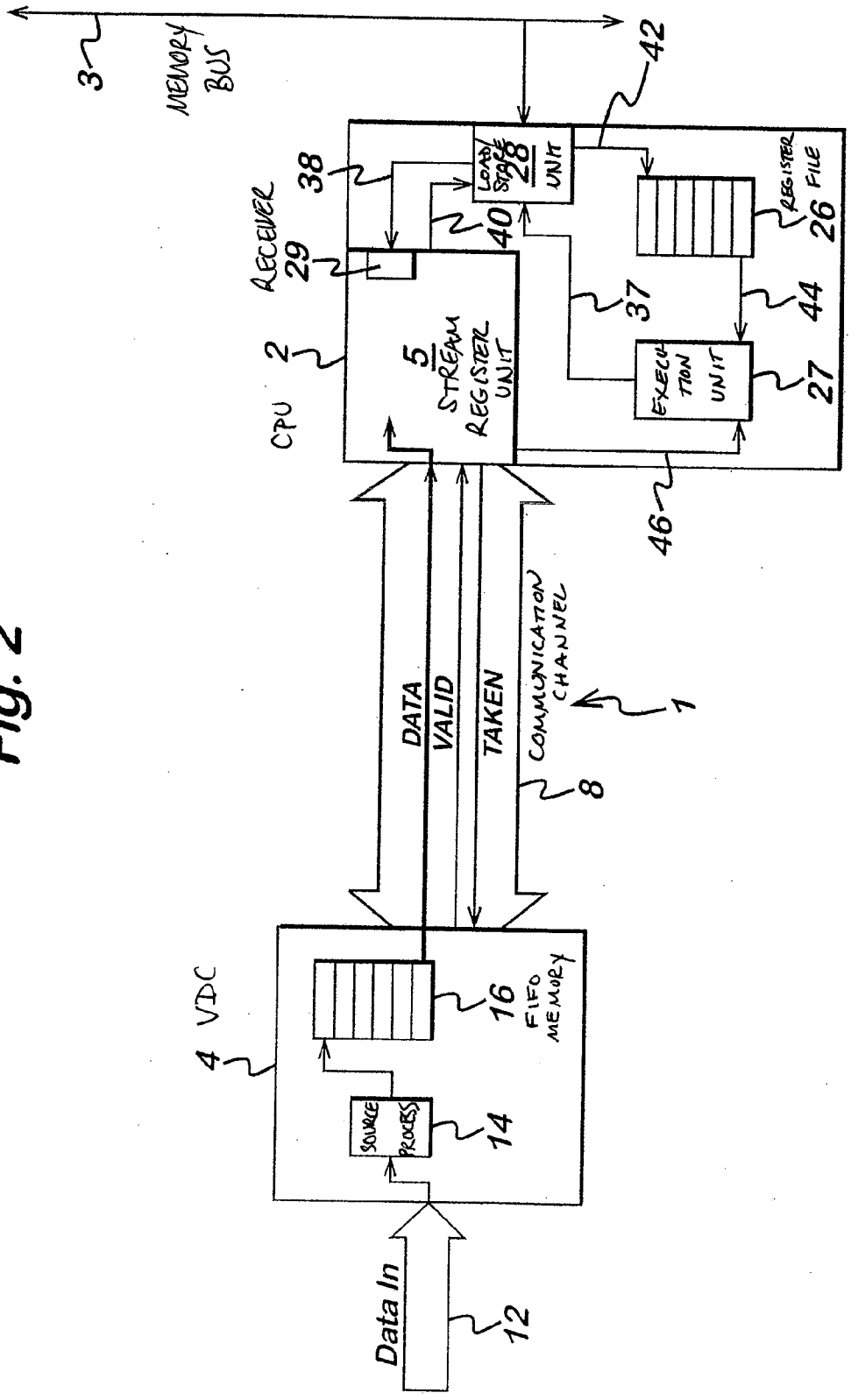
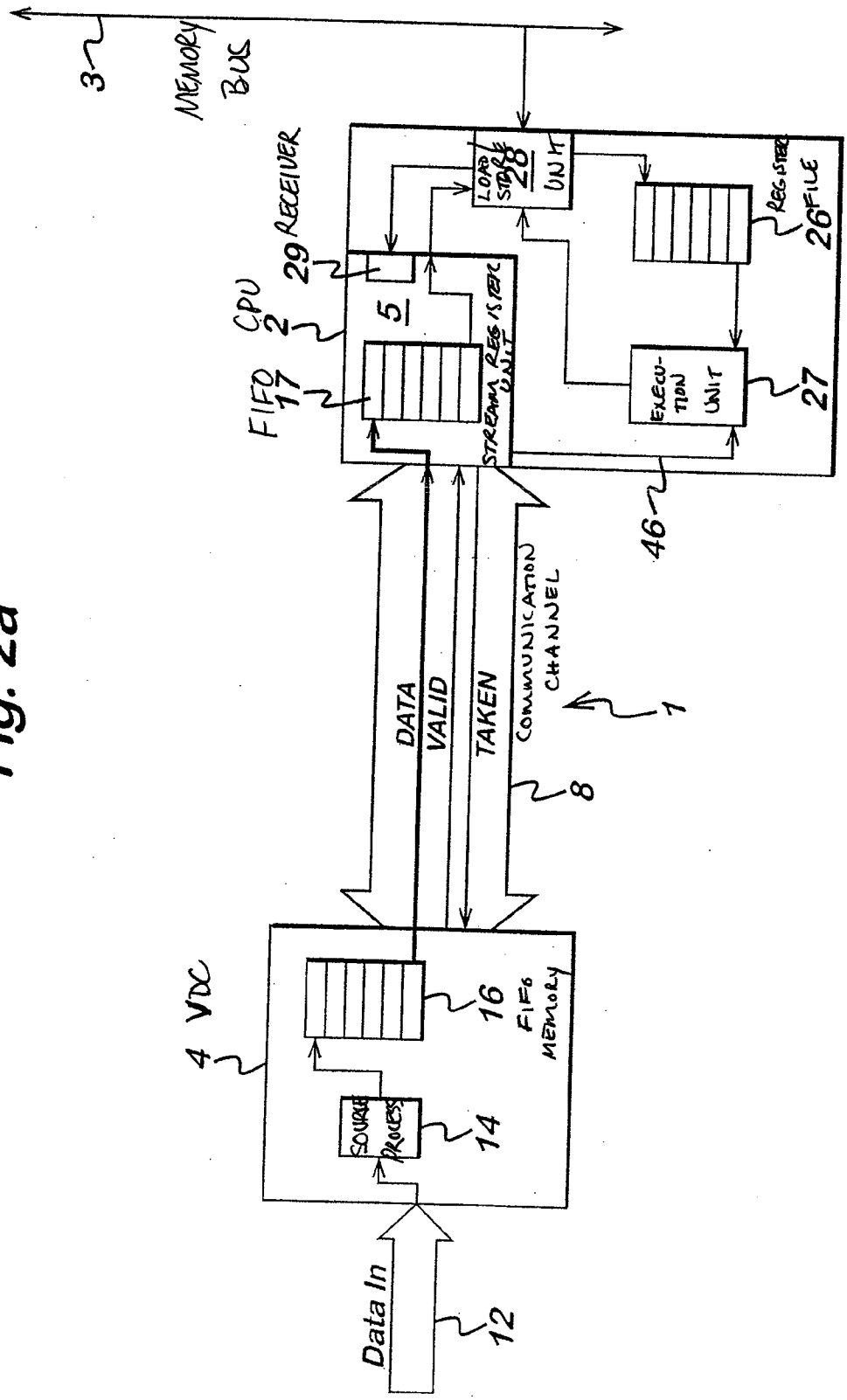

3
MEMORY BUS
42
LOAD/STORE UNIT
28
38
40
RECEIVER
29
REGISTER FILE
26
37
44
CPU
2
5
STREAM REGISTER UNIT
EXECUTION UNIT
27
46
DATA
VALID
TAKEN
COMMUNICATION CHANNEL
1
8
VDC
4
16
FIFO MEMORY
SOURCE PROCESS
14
Data In
12

Fig. 2

Fig. 2a


3
MEMORY BUS
CPU
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29 RECEIVER
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FIFO
17
STREAM REGISTER UNIT
LOAD STORE UNIT
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REGISTER FILE
26
EXECUTION UNIT
27
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COMMUNICATION CHANNEL
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SOURCE PROCESS
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Data In
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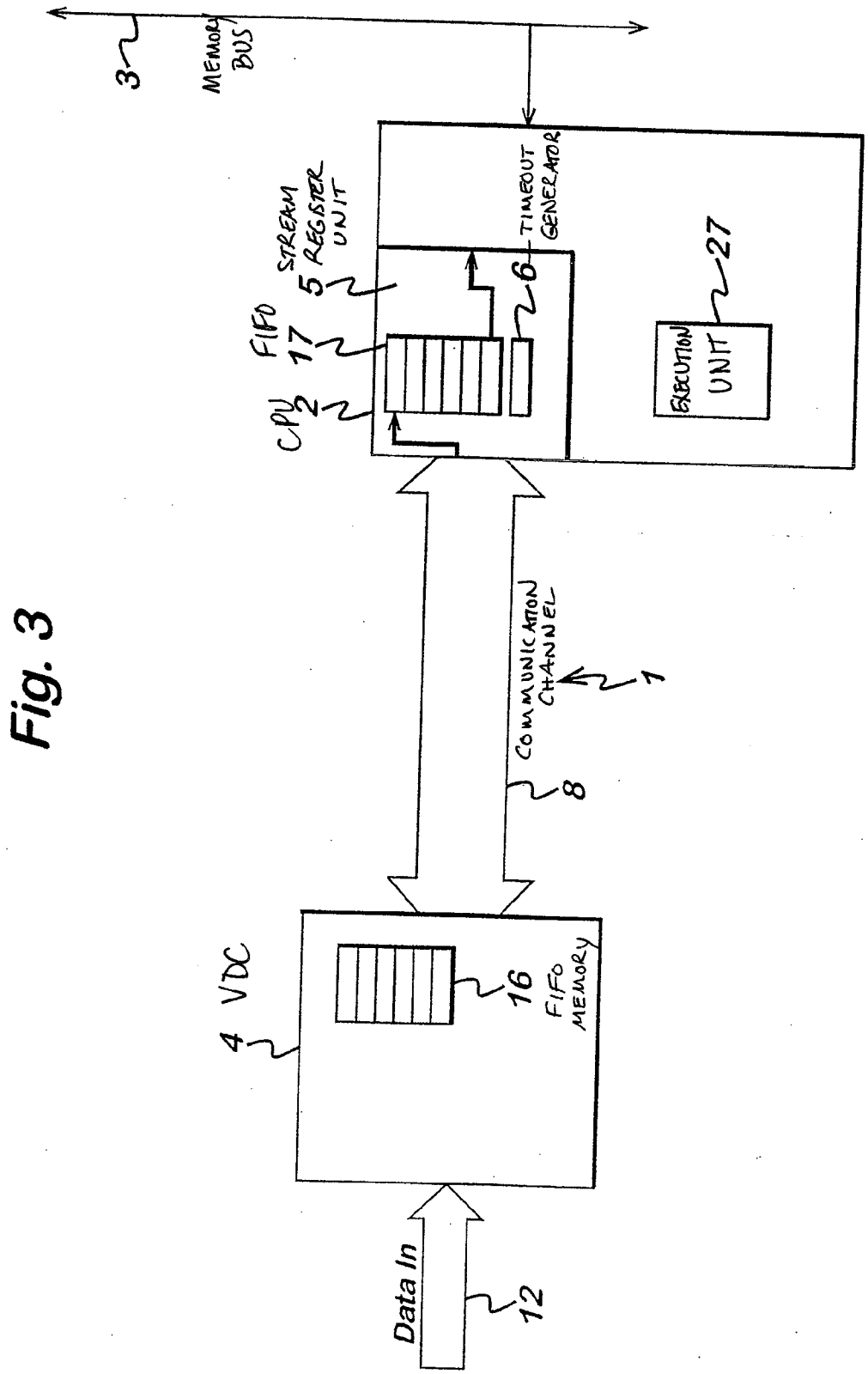
3
MEMORY BUS
STREAM REGISTER UNIT
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TIMEOUT GENERATOR
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27
FIFO
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CPU
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EXECUTION UNIT
COMMUNICATION CHANNEL
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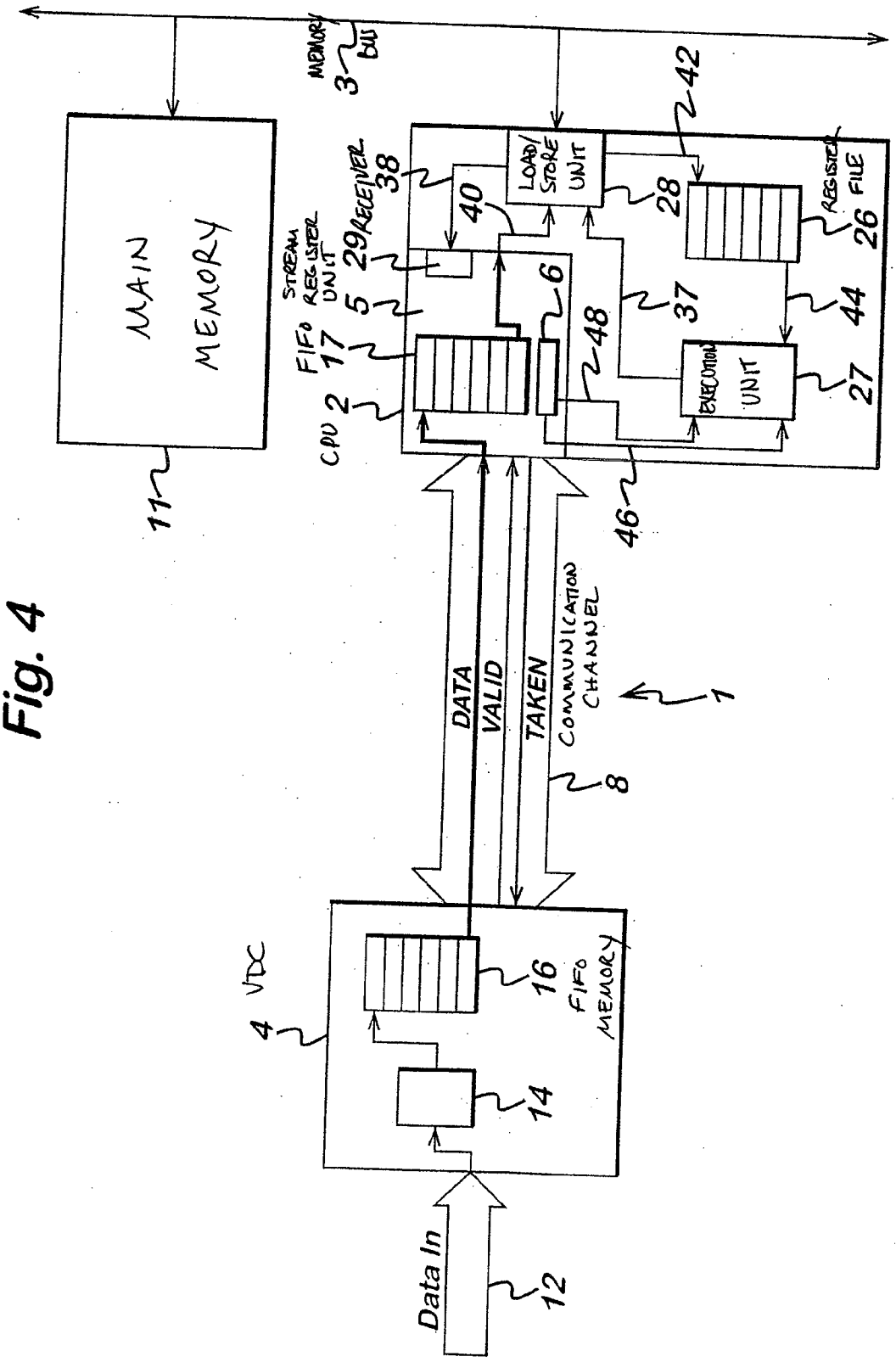
4 VDC
16
FIFO MEMORY
Data In
12

Fig. 3

Fig. 4


MEMORY BUS
3
MAIN MEMORY
11
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38
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6
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